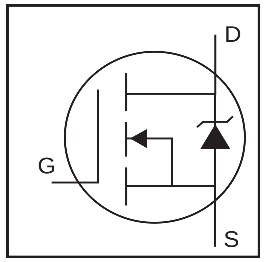
International
IOR Rectifier

PD- 91842A

IRLBA1304

HEXFET® Power MOSFET

- Logic-Level Gate Drive
- Ultra Low On-Resistance
- Same outline as TO-220
- 50% greater current in typ. application conditions vs. TO-220
- Fully Avalanche Rated
- Purchase IRLBA1304/P for solder plated option.



V_{DSS} = 40V

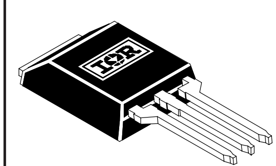
$R_{DS(on)}$ = 0.004Ω

I_D = 185A⑤

Description

The HEXFET® is the most popular power MOSFET in the world.

This particular HEXFET® is in the Super220™ and has the same outline and pinout as the industry standard TO-220. It has increased current handling capability over both the TO-220 and the much larger TO-247 package. This makes it ideal to reduce component count in multiparalled TO-220 applications, reduce system power dissipation, upgrade existing designs or have TO-247 performance in a TO-220 outline. This package has also been designed to meet automotive qualification standard Q101.



Super - 220

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	185, pkg limited to 95A*	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	130, pkg limited to 95A*	
I_{DM}	Pulsed Drain Current ①	740	
P_D @T_C = 25°C	Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy②	1160	mJ
I_{AR}	Avalanche Current①	100	A
E_{AR}	Repetitive Avalanche Energy①	30	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Recommended clip force	20	N

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.5	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	——	
$R_{\theta JA}$	Junction-to-Ambient	——	58	

* Current capability in normal application, see Fig.9.

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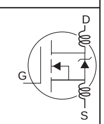
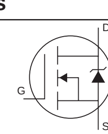
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.043	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.0040	Ω	V_{GS} = 10V, I_D = 110A ④
		——	——	0.0065		V_{GS} = 4.5V, I_D = 93 ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	——	——	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance	120	——	——	S	V_{DS} = 25V, I_D = 110A
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	μA	V_{DS} = 40V, V_{GS} = 0V
		——	——	250		V_{DS} = 32V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -16V
Q_g	Total Gate Charge	——	——	140	nC	I_D = 110A
Q_{gs}	Gate-to-Source Charge	——	——	39		V_{DS} = 32V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	79		V_{GS} = 4.5V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	——	21	——		V_{DD} = 20V
t_r	Rise Time	——	350	——		I_D = 110A
$t_{d(off)}$	Turn-Off Delay Time	——	45	——		R_G = 0.9Ω
t_f	Fall Time	——	103	——		R_D = 0.18Ω,See Fig. 10 ④
L_D	Internal Drain Inductance	——	2.0	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	——	5.0	——		
C_{iss}	Input Capacitance	——	7660	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	2150	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	460	——		ƒ = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	185*	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	740		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 110A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	100	150	ns	T_J = 25°C, I_F = 110A
Q_{rr}	Reverse RecoveryCharge	——	250	380	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 230μH R_G = 25Ω, I_{AS} = 100A. (See Figure 12)

③ I_{SD} ≤ 110A, di/dt ≤ 170A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

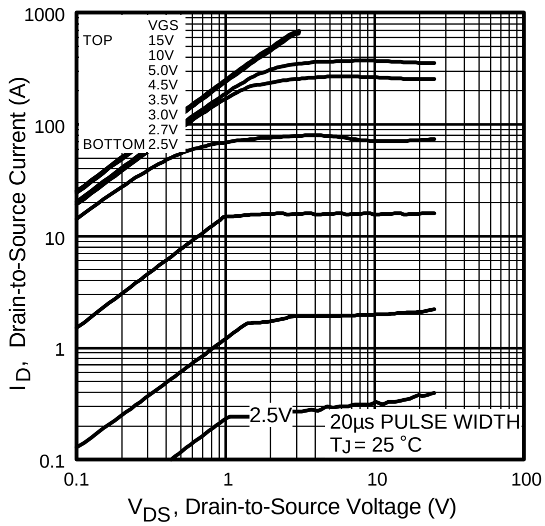


Fig 1. Typical Output Characteristics

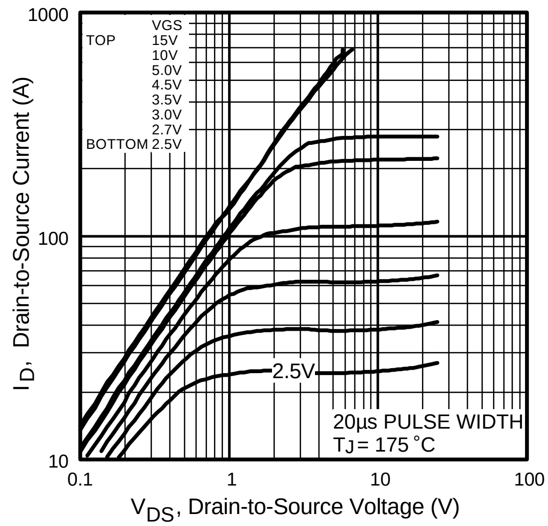


Fig 2. Typical Output Characteristics

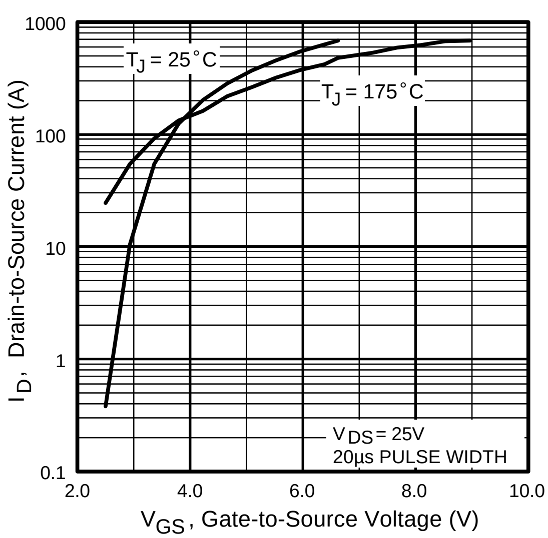


Fig 3. Typical Transfer Characteristics

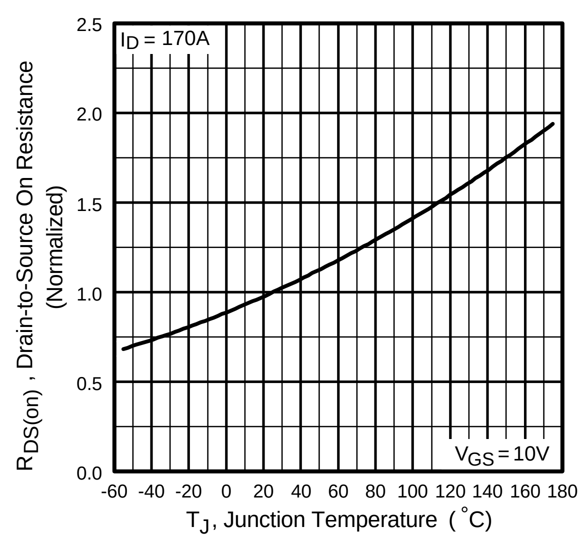


Fig 4. Normalized On-Resistance Vs. Temperature

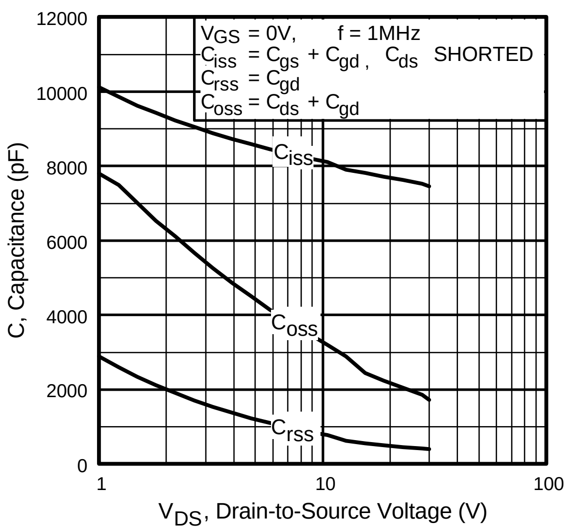


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

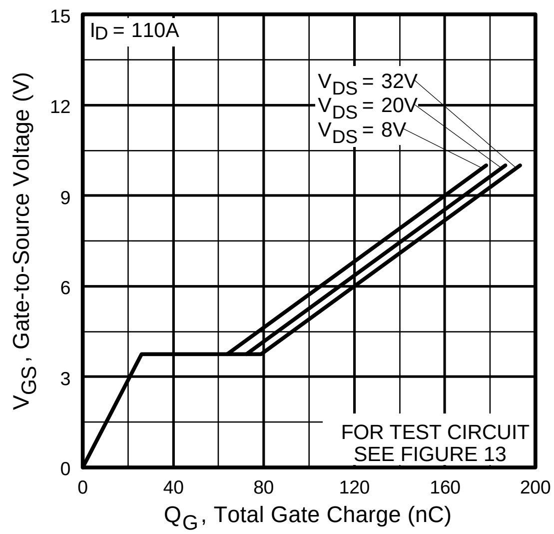


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

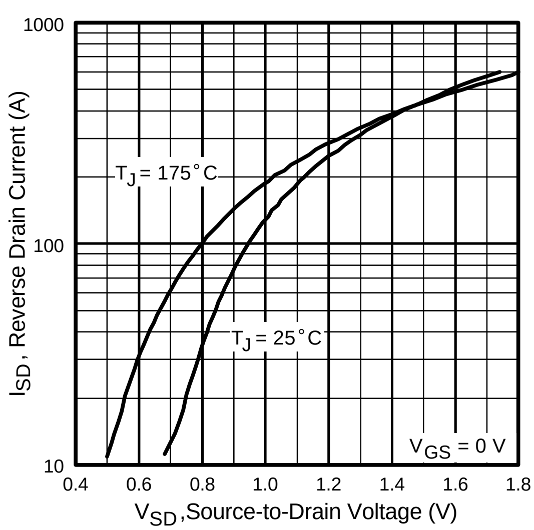


Fig 7. Typical Source-Drain Diode Forward Voltage

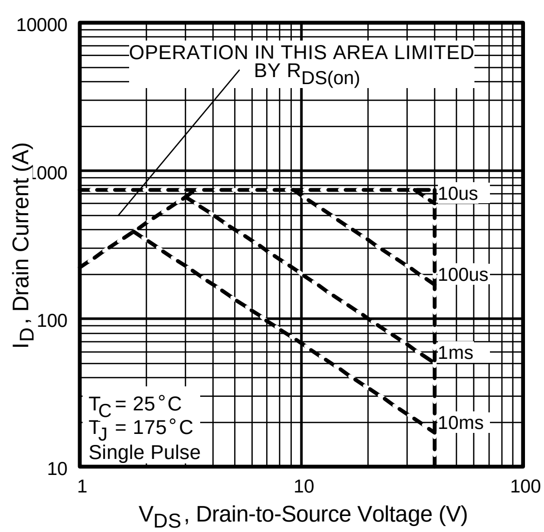


Fig 8. Maximum Safe Operating Area

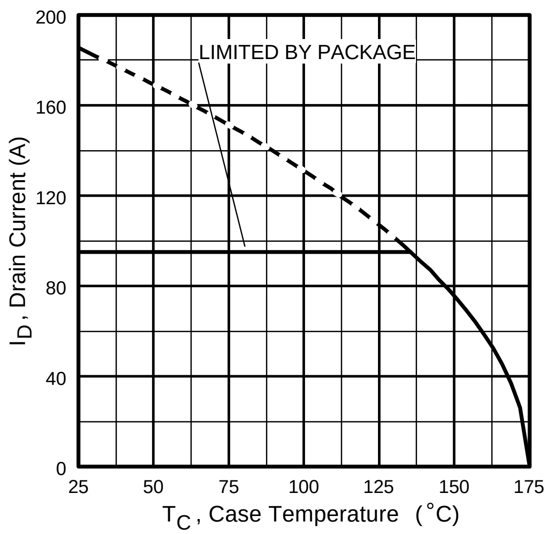


Fig 9. Maximum Drain Current Vs. Case Temperature

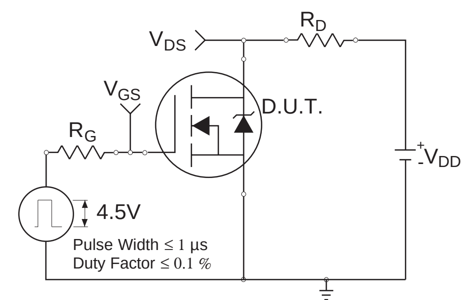


Fig 10a. Switching Time Test Circuit

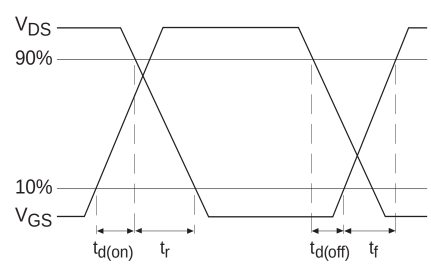


Fig 10b. Switching Time Waveforms

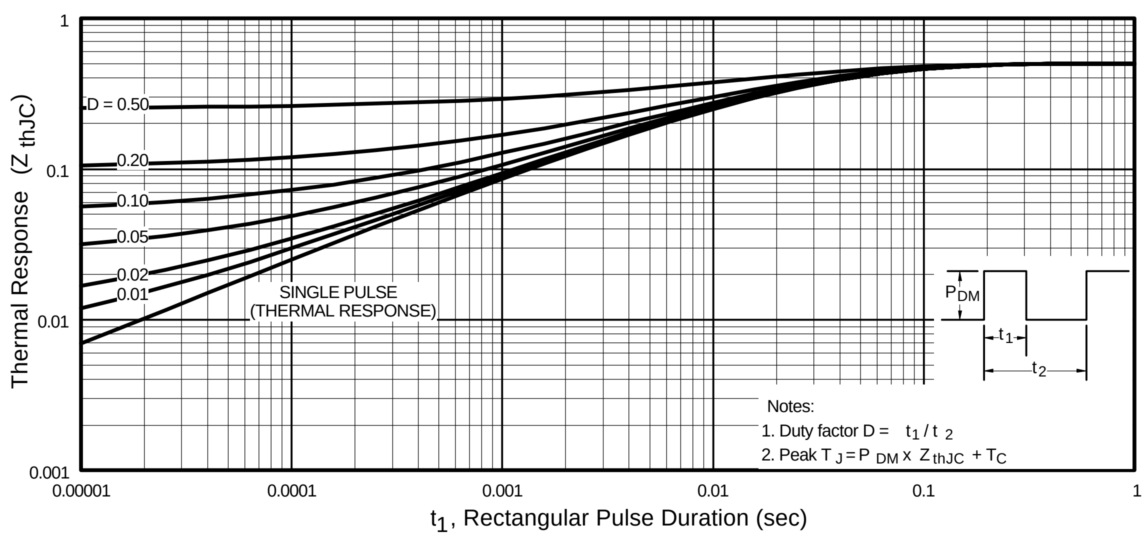


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

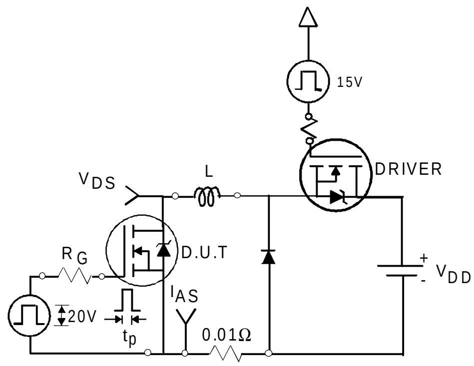


Fig 12a. Unclamped Inductive Test Circuit

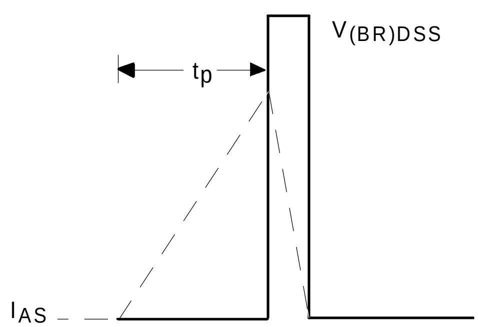


Fig 12b. Unclamped Inductive Waveforms

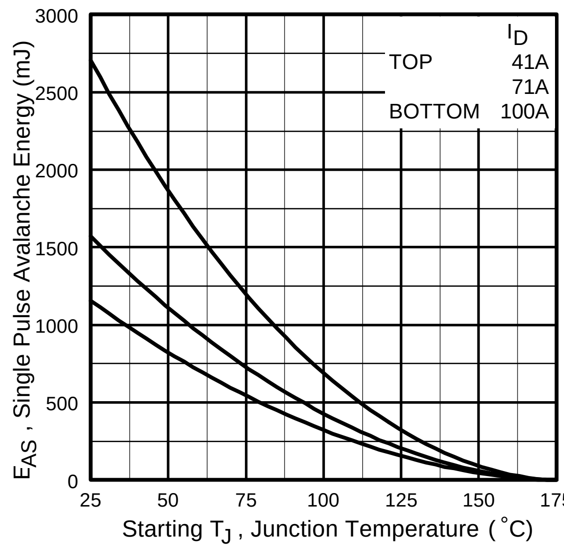


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

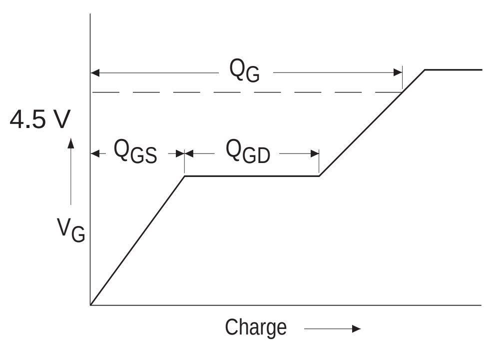


Fig 13a. Basic Gate Charge Waveform

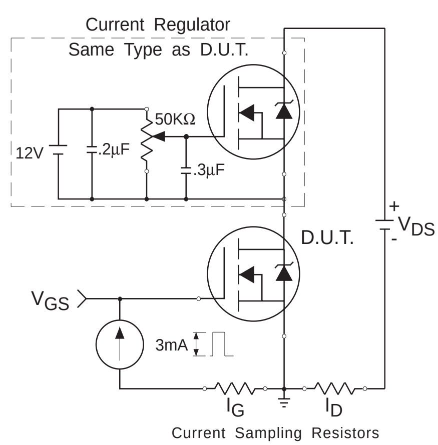
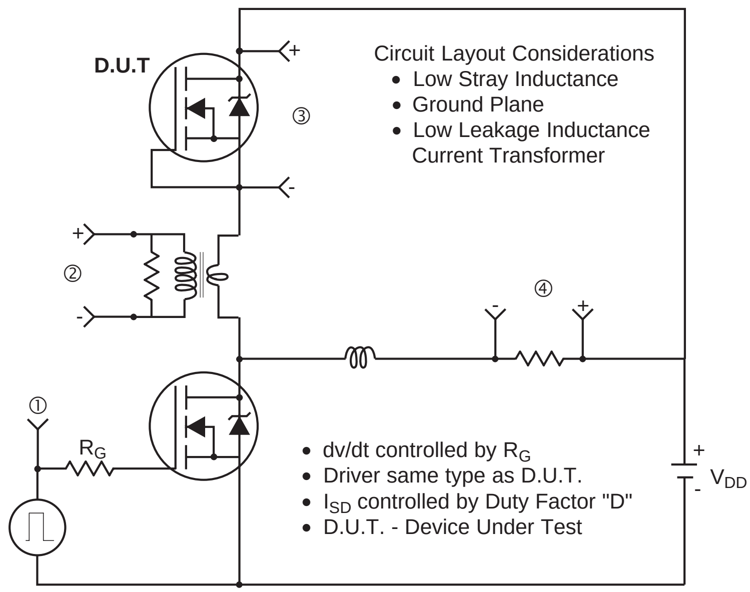
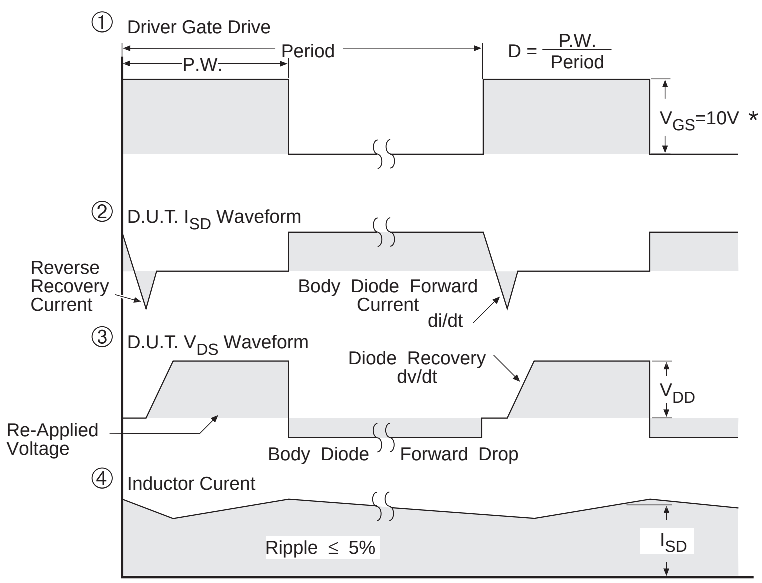


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

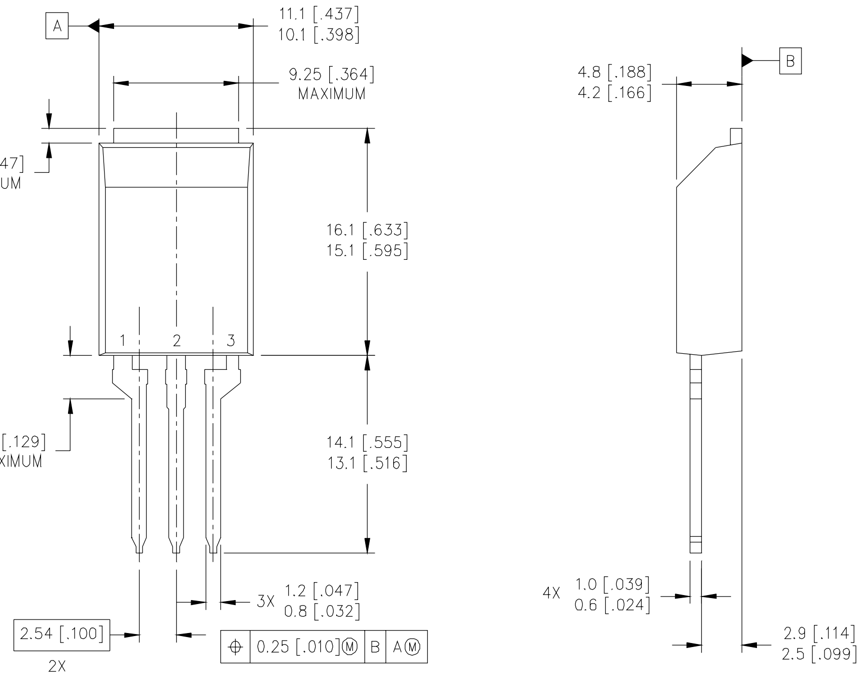




* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Super-220 Package Outline



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO–273AA.

LEAD ASSIGNMENTS

HEXFET	IGBT
1 – GATE	1 – GATE
2 – DRAIN	2 – COLLECTOR
3 – SOURCE	3 – EMITTER
4 – DRAIN	4 – COLLECTOR

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